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10/694,923	10/27/2003	Michael M. Klock	NVID-062/00US 140060-2128	5104

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EXAMINER	
WASHBURN, DANIEL C	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,923	KLOCK ET AL.	
	Examiner	Art Unit	
	DANIEL WASHBURN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,21,25 and 28-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,21,25 and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 3/25/04 have been fully considered but they are not persuasive.

As to the applicant's argument that none of the cited art describes actively monitoring a graphics pipeline, the examiner contests that Williams et al. (US 6,397,343) describes actively monitoring a graphics pipeline at 6:51-67, 7:1-20, and 8:11-22 (cited portions explained the rejection given below).

In response to applicant's argument that Bose et al. (US 7,076,681) is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Bose describes monitoring the activity of stages within a pipeline (i.e., detecting whether or not one or more stages is currently stalled) and adjusting the clock frequency of at least the stages following the stalled stage in order to conserve power, which is considered to be reasonably pertinent to the particular problem with which the applicant is concerned, as the applicant's claimed invention includes monitoring one or more stages of a pipeline in order to determine if the clock signals supplied to the pipeline should be increased or decreased, based on whether or not one or more stages are stalling a particular percentage of the time.

As to the applicant's argument that one of ordinary skill in the art at the time of the invention would understand that a graphics pipeline functions differently from a superscalar processor, the examiner contests that the concept of monitoring a pipeline in order to determine if one or more stages are stalling, and adjusting one or more clocks at the pipeline according to the result of the monitoring can easily be applied to any pipeline, regardless of whether it's a graphics pipeline, as disclosed in Williams, or a pipeline included as part of a superscalar processor, as disclosed in Bose.

As to the applicant's argument that stalling in Bose is completely unrelated to waiting for inputs from upstream stages, the examiner contests that Bose, at 6:36-60, describes that a few cycles after the I-unit stalls the I-pipe is empty, which means it has nothing for the E-unit. The I-unit stalling is considered to also stall the E-unit and any other units that follow the I-unit, thus, when the I-unit stalls this inherently means that the E-unit will stall, at which point the clock of the E-unit and any other units that follow the I-unit should be reduced in order to conserve power while waiting for inputs from one or more upstream stages.

As to the applicant's argument that Bose teaches away from the applicant's invention, as in Bose the detection of a stall in an E-unit results in an adjustment down of the clock speed in the upstream I-unit to reduce or cut off the rate at which instructions are received by the stalled E-unit; and thus in Bose a stall in a stage results in the stage requesting the upstream unit to reduce its clock rate to cut down the rate at which instructions are received, while in the claimed invention the performance level and hence the clock rate is increased in response to detecting a stall, the examiner

contests that the applicant's claims do not specify that the clock rate of the pipeline is increased in response to a detected stall. The applicant's claims recite, "determining whether the graphic pipeline is under-utilized or over-utilized based on the percentage of clock cycles for which there is a stall within the graphics pipeline; increasing the performance level (clock rate) in response to detecting an over-utilization condition and reducing the performance level (clock rate) in response to detecting an under-utilization condition." Thus, a stall in the pipeline is considered an under-utilization condition of the pipeline, which results in a reduced clock rate, and no stall in the pipeline is considered an over-utilization condition of the pipeline, which results in an increased clock rate. Therefore, Bose does not teach away from the applicant's invention as claimed.

Claim Objections

Claim 25 is objected to because of the following informalities: Claim 25 line 17 reads, "…increase a clock ***rate the*** graphics processor core clock domain…" the examiner assumes it should read, "…increase a clock ***rate in the*** graphics processor core clock domain…"

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 21, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giemborek et al. (US 6,950,105) in view of Williams et al. (US 6,397,343), and further in view of Bose et al. (US 7,076,681).

As to claim 1, Giemborek describes a method of operating a graphics system having a sequence of at least two discrete performance levels with each performance level being defined by a core clock rate of a graphics processing unit and a memory clock rate, the method comprising:

operating the graphics system at the core clock rate and memory clock rate associated with a selected performance level, the selected performance level being a minimum performance level sufficient to maintain the display rate within a normal range (column 1 lines 50-67 through column 2 lines 1-11 and Figure 1 describes graphics accelerator 10, which matches the speed of at least one of two or more clocks (e.g., engine clock 40 and memory clock 42) to levels (speeds) under software control to a rate sufficient to satisfy current display requirements. The graphics accelerator includes 2D/3D engine 20, overlay engine 22, and frame buffer 16. Further, column 7 lines 50-67 through column 8 lines 1-27 describes increasing the clock speeds of the clocks within the graphics accelerator 10 if the system is currently over-utilized and decreasing the clock speeds of the clocks within the graphics accelerator 10 if the system is currently under-utilized. Finally, column 1 lines 50-65 describes that the clock speeds are set such that display rate remains in a normal range (i.e., graphics display performance is not sacrificed)).

Giemborek doesn't describe monitoring utilization of a graphics pipeline.

However, Williams describes monitoring the utilization of a graphics pipeline.

Williams describes a method and system that includes a device for dynamic graphics subsystem clock adjustment within a computer system having a CPU and a dedicated graphics subsystem. A system interface is coupled to the graphics subsystem to allow a controller to determine the graphics processing load placed on the graphics subsystem (column 4 lines 11-31 and column 6 lines 33-50). Williams further describes that monitoring said at least one attribute (in this case the graphics processing load placed on the graphics subsystem) comprises: monitoring at least one attribute indicative of utilization of a graphics pipeline within a graphics processor core clock domain and determining whether the graphic pipeline is under-utilized or over-utilized (column 6 lines 51-67, column 7 lines 1-20, and column 8 lines 11-22 describes that the device 100 determines the graphics subsystem load by monitoring the processing activity of graphics subsystem 200 via the pipeline control 206 (e.g., by snooping graphics commands and data flowing through a graphics pipeline to determine the activity level of the graphics pipeline) and adjusts the pipeline clock frequency accordingly).

All the above-described limitations of claim 1 are known in Giemborek and Williams, the only difference is the combination of old elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Giemborek the system and method of determining the processing load placed on a graphics subsystem by monitoring the level of activity of a

graphics pipeline, and adjusting the frequency of the pipeline clock according to the determined load, as taught by Williams, as this doesn't change the operation of the rest of the system, and it could be used to achieve the predictable results of improving the efficiency of the 2D/3D graphics engine disclosed in Giemborek by monitoring the pipeline activity within the graphics engine and determining a required clock rate to be passed to the engine based, in part, on the monitored activity. One advantage of passing the graphics engines a variable clock rate based at least in part on calculated activity within a pipeline within the engine is that the system can further reduce its power consumption and optimize its calculated clock rates by adding the activity of the pipeline to the list of factors that are used when determining the clock rates.

Giemborek in view of Williams doesn't describe monitoring a percentage of clock cycles at one or more points within a graphics processor core clock domain for which one or more stages of a graphics pipeline are stalled waiting for inputs from upstream stages as an indicator of utilization and determining whether the graphic pipeline is under-utilized or over-utilized based on the percentage of clock cycles for which there is a stall within the graphics pipeline; and

However, Bose describes an integrated circuit such as a scalar processor. Circuit components or units are clocked by and synchronized to a common system clock. A local clock generator in each clocked unit combines the common system clock and stall status from one or more other units to adjust the register clock frequency up or down (column 3 lines 52-62). Bose further describes (column 6 lines 36-60 and Figure 2) an example that includes an instruction unit (I-unit) and an execution unit (E-unit), the I-unit

and E-unit include activity monitoring and clock control logic 126, 128, respectively, which monitor unit activity level. When the E-unit 124 senses a stall condition it asserts a stall bit 130, which is used to adjust down the clock speed of the I-unit clock (to throttle down the I-unit and effectively reduce the instruction rate to the E- unit). Depending on the granularity of the control the E-unit activity status or stall bit 130 can adjust its own clock within the E-unit. When the E-unit stall ends the I-unit clock is throttled back up to its normal clock rate. Similarly, when the I-unit experiences a stall condition it sends an I-pipe empty bit to the E-unit so the E-unit can adjust down its clock to conserve power. The activity monitoring and clock control logic 126, 128 contained within each stage of the scalar processor is considered to monitor the percentage of clock cycles at one or more points within a graphics processor core clock domain for which one or more stages (e.g., the E-unit) of a graphics pipeline are stalled waiting for inputs from upstream stages (e.g., the I-unit) as an indicator of utilization and determining whether the graphic pipeline is under-utilized or over-utilized based on the percentage of clock cycles for which there is a stall within the graphics pipeline. In this case when the percentage of clock cycles for which the E-unit is held up waiting for the results of the I-unit is greater than zero the activity monitoring and clock control logic within the I-unit notifies the E-unit stage to reduce its clock speed in order to conserve power until the stalling I-unit overcomes the stall. The stall at the I-unit is considered an under-utilized condition of the pipeline, as a stage of the pipeline is stalling, which means all stages at least from that stage on are also stalling, and which further means that a maximum clock rate for at least the stalling stages in unnecessary. No stall at the

I-unit is considered an over-utilized condition of the pipeline, as the pipeline should be operating at its maximum rate, which means the E-unit clock needs to be set to its maximum rate in order to keep up with the incoming data.

Further, increasing the clock rate of the E-unit when the stall at the I-unit has ended is considered increasing the performance level in response to detecting an over-utilization condition to increase the clock rate in the graphics processor core clock domain, and decreasing the clock rate at the E-unit when a stall occurs at the I-unit is considered decreasing the performance level in response to detecting an under-utilization condition to decrease the clock rate in the graphics processor core clock domain.

All the elements of claim 1 are known in Giemborek in view of Williams and further in view of Bose, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Giemborek in view of Williams the system and method of monitoring a percentage of clock cycles at one or more points within a graphics processor core clock domain for which one or more stages of a graphics pipeline are stalled waiting for inputs from upstream stages as an indicator of utilization and determining whether the graphic pipeline is under-utilized or over-utilized based on the percentage of clock cycles for which there is a stall within the graphics pipeline; and increasing the performance level in response to detecting an over-utilization condition to increase the clock rate in the graphics processor core clock domain and decreasing the

performance level in response to detecting an under-utilization condition to decrease the clock rate in the graphics processor core clock domain, as taught by Bose, in order to achieve the predictable result of improving the efficiency and power conservation of the 2D/3D graphics engine (disclosed in Giemborek) by monitoring the pipeline activity within the graphics engine and determining a clock rate for each stage within the pipeline. The advantage of assigning a clock rate to each stage within the pipeline, rather than simply passing them a single clock rate, is that the system can further reduce its power consumption by adjusting the clock rate of stages that are waiting for the results of another stage in order to conserve power at those stage until the stalling stage produces its result.

Concerning claim 21, Giemborek describes a method of operating a graphics system having a sequence of at least two discrete performance levels where each performance level is defined by a core clock rate of a graphics processing unit and a memory clock rate, the performance levels including a high performance level for processing complex three-dimensional graphical images and at least one lower power, lower performance level for processing less complex graphical images, the method comprising:

operating the graphics system at the core clock rate and memory clock rate associated with the selected performance level, the selected performance level being a minimum performance level sufficient to maintain the display rate within the normal range (see the corresponding section in the rejection of claim 1).

Giemborek doesn't describe but Williams describes monitoring the utilization of a graphics pipeline (see the corresponding section in the rejection of claim 1).

Giemborek in view of Williams doesn't describe but Bose describes monitoring a percentage of clock cycles at one or more points within a graphics processor core clock domain for which one or more stages of a graphics pipeline are stalled waiting for inputs from upstream stages as an indicator of utilization and determining whether the graphic pipeline is under-utilized or over-utilized based on the percentage of clock cycles for which there is a stall within the graphics pipeline (see the corresponding section in the rejection of claim 1);

in response to detecting a level of utilization greater than an over-utilization threshold for which a display rate of the graphics system is likely to be significantly decreased below a normal display rate, selecting a higher performance level to increase a clock rate in the graphics processor core clock domain (6:36-60 describes that when the E-unit detects that a stall in the I-unit has ended the clock rate of the E-unit is throttled back up, which is considered detecting a level of utilization greater than an over-utilization threshold for which a display rate of the graphics system is likely to be significantly decreased below a normal display rate, as the level of utilization of the pipeline is back up to maximum utilization, which means the clock rate of the E-unit must be throttled back up in order to keep up with the instruction flow from the I-unit, which is considered selecting a higher performance level to increase a clock rate in the graphics processor core clock domain); and

in response to detecting a level of utilization below an under-utilization threshold, selecting a lower performance level to reduce the clock rate in the graphics processor core clock domain to reduce power required by the graphics system (6:36-60 describes that when the E-unit detects that a stall has occurred in the I-unit, the E-unit throttles down its clock, which is considered detecting a level of utilization below an under-utilization threshold (the I-unit is stalled, which reduces the utilization of the pipeline), and in response selecting a lower performance level to reduce the clock rate in the graphics processor core clock domain to reduce power required by the graphics system (the reduced clock rate in the E-unit is considered a lower performance level that reduces the power required by the graphics system).

See the rejection of claim 1 for rationale to combine Bose with Giemborek and Williams.

As to claim 25, Giemborek describes a graphics system, comprising:

a graphics processor having a sequence of at least two discrete performance levels where each performance level is defined by a graphics processor core clock rate of a graphics processing unit and a memory clock rate (column 1 lines 50-67 through column 2 lines 1-11 and Figure 1 describes graphics accelerator 10, which matches the speed of at least one of two or more clocks (e.g., engine clock 40 and memory clock 42) to levels (speeds) under software control to a rate sufficient to satisfy current display requirements. The graphics accelerator includes 2D/3D engine 20, overlay engine 22, and frame buffer 16); and

a graphics memory coupled to said graphics processor by a graphics bus and operable at said memory clock rate (Figure 1 and column 2 lines 27-36 describes frame buffer memory 16);

the graphics system operating at the core clock rate and memory clock rate associated with the performance level selected by the performance level controller, the selected performance level being a minimum performance level capable of maintaining the display rate within a normal range (column 1 lines 50-65 describes that the clock speeds are selected to ensure that the graphics display performance is not degraded).

Giemborek doesn't describe but Williams describes monitoring the utilization of a graphics pipeline (see the corresponding section in the rejection of claim 1).

Giemborek in view of Williams doesn't describe but Bose describes a performance level controller (6:36-60 describes activity monitoring and clock control logic 126, 128, which are collectively considered the performance level controller), said performance level controller configured to monitor, as a function of time, a percentage of clock cycles at one or more points within a graphics processor core clock domain for which one or more stages of a graphics pipeline are stalled waiting for inputs from upstream stages as an indicator of utilization and determining whether the graphic pipeline is under-utilized or over-utilized based on the percentage of clock cycles for which there is a stall in the graphics pipeline (see the corresponding section in the rejection of claim 1); and

said performance level controller configure to increase said performance level to increase a clock rate in the graphics processor core clock domain and to avoid over-

utilization of said graphics pipeline (6:36-60 describes that when the stall in the I-unit ends the pipeline should be operating at maximum speed again, which means the clock rate of the E-unit needs to be increased (considered increasing the performance level) to avoid over-utilization of the graphics pipeline (the increase in clock speed ensures that all stages of the pipeline will be able to keep up with the flow of data)).

said performance level controller configured to decrease said performance level from a high performance level to a lower performance level to decrease the clock rate in the graphics processor core clock domain to avoid under-utilization of said graphics pipeline (6:36-60 describes that when a stall condition occurs in the I-unit the clock for the E-unit is throttled down (considered decreasing the performance level), which ensures that the pipeline isn't needlessly wasting power and thus being under-utilized).

See the rejection of claim 1 for rationale to combine Bose with Giemborek and Williams.

Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giemborek et al. (US 6,950,105) in view of Williams et al. (US 6,397,343) in view of Bose et al. (US 7,076,681), as applied to claims 1, 21, and 25 above, and further in view of Culbert et al. (US 6,820,209).

As to claims 28-30, Giemborek describes a 2D/3D graphics engine that is capable of operating at different clock speeds (column 2 lines 42-67), where the 2D/3D graphics engine is operated at a speed that is determined based on factors that include the software running on a host CPU, as well as display mode settings of the computer,

such as screen resolution, pixel or color depth, and screen refresh rate (column 5 lines 13-48).

Giemborek in view of Williams and further in view of Bose doesn't describe the method of claims 1, 21, or 25 wherein said at least two discrete performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level.

However, Culbert describes a system and method wherein at least two discrete performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level (column 5 lines 46-67 through column 6 lines 1-43 describes a system that includes a 2D graphics engine 212 and a separate 3D graphics engine 214. The 2D and 3D graphics engines are only activated when the graphics controller needs to produce 2D or 3D graphics. Further, column 6 lines 44-67 through column 7 lines 1-16 describes that the graphics controller supplies a clock signal to the 2D engine and a second clock signal to the 3D engine. To reduce power consumption, the clock signal normally sent to the 2D engine is stopped when the 2D engine is not being utilized, and likewise the clock signal normally sent to the 3D engine is stopped when its processing resources are not being utilized. Thus, Culbert is considered to describe a low power two-dimensional graphics performance level (when the 2D processor isn't being

utilized), a standard two-dimensional graphics performance level (when the 2D processor is being utilized), a low-power three-dimensional graphics performance level (when the 3D processor isn't being utilized), and a high performance three-dimensional graphics performance level (when the 3D processor is being utilized)).

All the elements of claims 28-30 are known in Giemborek, Williams, Bose, and Culbert, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Giemborek in view of Williams and further in view of Bose the system and method wherein said at least two discrete performance levels include a low power two-dimensional graphics performance level, a standard two-dimensional graphics performance level, a low power three-dimensional graphics performance level, and a high performance three-dimensional graphics performance level, as taught by Culbert, as a system and method wherein the 2D engine is separate from the 3D engine, and where each engine is separately controlled, could be used to achieve the predictable result of more effectively saving power, as when only the 2D or only the 3D engine is required for a particular operation, the other engine can be powered down, which doesn't degrade the performance of the system, and reduces power consumption even more than clocking the 2D and 3D engines up and down together (as described in Giemborek).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Oliver et al. (US 7,243,217) describes a floating point unit that increases its clock speed when an integer unit is stalled while waiting for an output from the floating point unit and decreases its clock speed when the integer unit is not waiting for an output from the floating point unit.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL WASHBURN whose telephone number is (571)272-5551. The examiner can normally be reached on Monday through Friday 8:30 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571) 272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ulka Chauhan/
Supervisory Patent Examiner, Art Unit 2628

/Dan Washburn/
Examiner, Art Unit 2628
7/11/08